UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,677	12/14/2005	Roger Cuppens	NL 030715	8560

65913 7590 11/06/2007

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
YANG, HAN	

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
11/06/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/560,677	CUPPENS, ROGER	
	Examiner	Art Unit	
	Han Yang	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *December 14th, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *December 14th, 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Search History*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-5, 7-10** are rejected under 35 U.S.C. 102(b) as being anticipated by **Keshtbod** (US Patent 4,527,255).

3. ***Regarding Independent claim 1***, Keshtbod teaches a static memory (**Fig. 2, Q1, Q2**) defining at least first and second nodes (**Fig. 2, N1, N2**) communicatively connected with read and/or write data lines (**Fig. 2, #23, #24**);

at least one non-volatile memory (**Fig. 2, Q3, Q4**) associated with the static memory (**Fig. 2, Q1, Q2**), and writing data stored therein to the static memory (**Fig. 2, Q1, Q2**);

the non-volatile memory (**Fig. 2, Q3, Q4**) comprising a first non-volatile element (**Fig. 2, Q3**) having a control gate connected to a first node (**Fig. 2, N2**) and a source connected to a second node (**Fig. 2, N1**), and a second non-volatile element (**Fig. 2, Q4**) having a control gate connected to the second node (**Fig. 2, N1**) and a source connected to the first node (**Fig. 2 N2**), the drain of each non-volatile element (**Fig. 2, Q3, Q4**) being connected by of a respective transistor (**Fig. 2, Q5, Q6**) to a supply voltage;

characterized in that the respective transistors (**Fig. 2, Q5, Q6**) are arranged to isolate

the drains (**Fig. 2 D3, D4**) of the first and second non-volatile elements from the supply during a program cycle of the memory device (**Fig. 2, #30**).

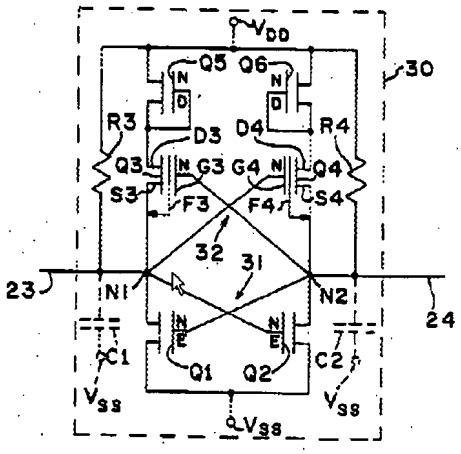

Fig. 2

4. ***Regarding claim 2***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise embedded flash or EEPROM elements (**Abstract, lines 3-5**).

5. ***Regarding claim 3***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise double or single poly floating gate type memory cells (**Abstract, lines 3-5**).

6. ***Regarding claim 4***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise devices, which can be programmed and erased by of tunneling of charges (**column 4, lines 58-61**).

7. ***Regarding claim 5***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) are programmed with opposite data (**column 7 lines 1-3, 13-15**).

8. ***Regarding claim 7***, Keshtbod teaches one or more respective selection

transistors (**Fig. 1, Q7, Q8**) are provided, by of which the nodes (**Fig. 1, Fig. 2, #23, #24**) are communicatively coupled to the read and/or write lines (**Fig. 1**).

9. ***Regarding claim 8***, Keshtbod teaches respective selection transistors (**Fig. 1, Q7, Q8**) are including one or more isolation transistors (**Fig. 1, Q7, Q8**).

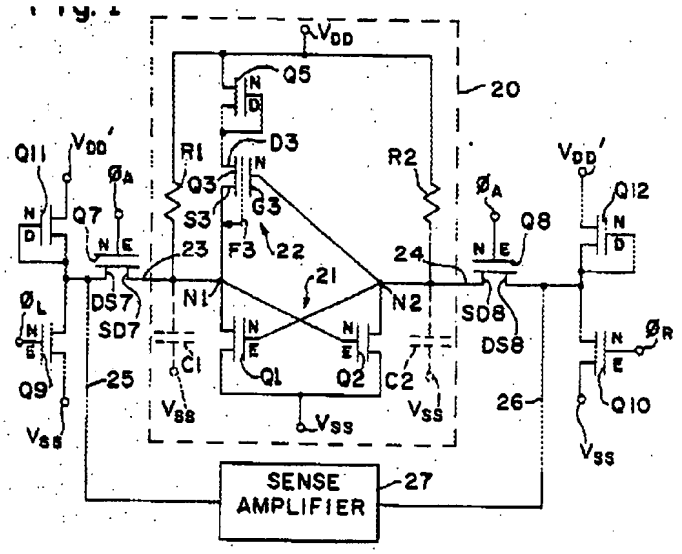

Fig. 1

10. ***Regarding claim 9***, Keshtbod teaches reconfigurable programmable logic device (**Fig. 4, column 10, lines 8-16**).

11. ***Regarding claim 9***, Keshtbod teaches a field programmable gate array including a memory device (**Fig. 4, column 10, lines 8-16**).

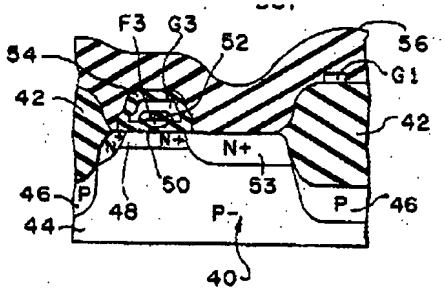

Fig. 4

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Keshtbod** (US Patent 4,527,255).

14. ***Regarding claim 6***, Keshtbod teaches the static memory (**Fig. 2, Q1, Q2**) comprises a pair of cross-coupled transistors

Keshtbod is silent with respect to the static memory (**Fig. 2, Q1, Q2**) comprises a pair of cross-coupled inverters.

The examiner takes **OFFICAL NOTICE** that cross-coupled transistors is functionally equivalent to cross-coupled inverter. Either of the cross-coupled static memory design is very common practice in the industrial world. However the cross-coupled transistors design would provide smaller size for the memory chip, since cross-coupled transistors only used four transistors per memory cell.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, Herdt (US Patent: 6,414,873), Lin et al. (US Patent 6,304,482)

Herdt (US Patent: 6,414,873) shows the static memory with flash memory.

Lin et al. (US Patent 6,304,482) shows the cross-coupled static memory design.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Han Yang whose telephone is (571) 270-0348. The examiner can normally be reached on Monday-Friday 8am-5pm with alternate Friday off. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1896. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HY

10/16/2007

ANH PHUNG
PRIMARY EXAMINER